AMENDMENT TO CLAIMS

1-48. (Cancelled)

49. (New) A processor that executes instructions converted by a compiler, comprising:

a fetching unit configured to fetch instruction packets one by one, wherein each instruction packet has fixed bit length and includes a plurality of instructions, wherein each instruction has a boundary information bit, a value of which indicates whether the instruction should be processed together with a succeeding instruction; and

an execution unit configured to process an instruction contained in a certain instruction packet and another instruction contained in a succeeding instruction packet in parallel based on the value of the boundary information bit,

wherein at least one of the instruction packets includes instructions which are processed sequentially, and

wherein the value of the boundary information bit is determined by the compiler during static parallel scheduling.

50. (New) The processor of claim 49, wherein the execution unit is further operable to process the instruction contained in the certain instruction packet and the another instruction contained in the succeeding instruction packet sequentially based on the boundary information.

51. (New) The processor of claim 50, wherein the processor is capable of executing a variable number of instructions in parallel.

52. (New) The processor of claim 51, wherein a bit length of instructions which the processor executes in parallel is variable.

53. (New) The processor of claim 49, further comprising:

an instruction buffer for temporally storing instructions so as to be executed in a later cycle.